Discussion on Design of Electromagnetic Compatibility of Digital Circuit PCB

Printed circuit board (PCB) is the most basic part of electronic equipment, it is a "bridge" between a ariety of electronic components and the electrical connection With the rapid development of electronic technology, people given the function on the PCB is more and more powerful, components and printed circuit density is getting higher and higher, with the resulting electromagnetic compatibility issues are more prominent. To make the best performance of electronic equipment, , in addition to the correct component selection and optimization of the circuit design, the good PCB electromagnetic compatibility design can also play a multiplier effect.

The application of digital circuit in modern electronic devices has been popular, and the problem of interference and anti-interference cannot be ignored. In this paper, only the digital circuit PCB electromagnetic compatibility design of the existence of the general issues are discussed.

Identify key circuits

Experience has proved that more than 90% of the electromagnetic interference (EMI) problem is caused by about 10% of the key circuit, as long as the correct identification and focus on the design of key circuits can prevent a lot of EMI problems.

For transmission, the biggest interference is high-speed repetition of the signal, Such as clock signals and bus signals, these signals are rich in high harmonics, it is a ready-made high-frequency "emission source" and easy to produce noise. Therefore, devices such as clock generators, crystal oscillators, and digital signal processors (DSPs) are placed close to each other and away from logic circuits to keep the DC / DC devices away from easily disturbing signal lines.

For the sensitivity problem, the biggest interference is reset line, interrupt line and control line. If these circuits are disturbed, the whole system may be in chaos. This problem can be prevented by adding a decoupling or filter circuit. Input / output (I / O) circuits are also critical for transmission and immunity, as they are connected to the outside and are likely to act as antennas and radiate outward.

Pay attention to the EMI problem when selecting the device

Without changing the logic circuit, selecting a low-rate device can help reduce the transmit interference. For example, when the 5MHz clock frequency increases to 15MHz, the emission will increase by a factor of three. In the design improvement, the choice of high-speed devices are as much as possible with the original pin-compatible, which can improve efficiency.

Due to the consumption of the peak current,High-speed CMOS circuit will cause serious harmonic transmission in the VCC line, application must be in the COMS circuit VCC between the ground

to increase the decoupling capacitor or add a small ferrite beads and VCC in series .High-speed CMOS devices, a small damping resistor (10 ~ 47Ω) is connected in series at the output to solve the "ringing" phenomenon caused by excessive signal lines. Usually the clock generator, crystal and CPU clock input are easy to produce noise and to be close to each other. Relays, high current switches and DC / DC switching power supply will bring interference, to be reasonable to separate, so that the coupling between each other smaller.

Circuit board selection

Using a multi-layer printed circuit board with a ground plane (all-ground plane), the EMI problem will be greatly improved. If from two layers of printed circuit board to multi-layer design, its performance will be improved several times.

Experience has shown that when the clock frequency is greater than 5MHz or pulse rise time is less than 5ns and suitable for multi-layer printed circuit board. For multilayer boards, the power plane and the ground plane should be close to each other, and one of them as a full ground plane can reduce the ground impedance. The key line is best placed in the inner layer, the general signal line can walk in the outer layer.

For digital circuits, double-layer printed boards are preferentially used to fill the area on the printed circuit board with ground grid or dot matrix wiring,so that can reduce the ground impedance, ground circuit and signal loop. Paying attention to the key lines (such as clock, reset line, etc.) are close to the loop to simulate the multi-layer board.

The initial wiring selection

Key signal lines are preferred. Power, high-speed signals, clock signals and synchronization signals and other key signals are given priority, and as soon as possible to provide a separate wiring layer. The layout of the function are grouped by function,, the high-speed circuit and low-speed circuit, high voltage and low voltage, digital circuit and analog circuit separate layout. Paying special attention to the oscillator and the crystal keep the distance between the external I / O circuit, the internal cable and the connector at least 25.4mm.

To use the manual cloth key line, after the completion of automatic wiring, be sure to carefully check the direction of the key line, and as short as possible.

For high-frequency circuits should pay atention to the termination of the printed circuit, usually the printed circuit board length is greater than 50mm / ns rise time when the need for termination, the typical termination is in parallel on the line R or RC, series R, parallel diode and so on.

Note the power supply decoupling

In a digital circuit, when the circuit are from one state to another state, it will produce a large peak

voltage on the power line to form a transient noise voltage. Local decoupling can reduce power line noise interference, the principle is: Connecting the 10 ~ 100μF tantalum capacitor to the high-frequency capacitor in parallel with the high-frequency capacitor; For digital processing devices, the high-frequency decoupling capacitors must be connected at the nearest power supply pin; To pay special attention to high-speed COMS devices, in general, The value of the capacitor value in the range of 0.01 ~ 0.1μF are the best, and to maintain the shortest lead.

Keeping the capacitor lead short enough, at high frequencies, the capacitor leads have a self-inductance, which forms a series resonant circuit , resulting in high-frequency parasitic oscillation, and should try to use the surface mount device. (SMT).

Noting the connector

Printed board connectors should be as remote as possible, such as clocks, power transformers and other radiation sources, but also away from reset or interrupt control circuits.

Reasonably place return line on the connector, making the signal path and return lines to be minimum ring, avoiding potential antenna ring. The key lines should be placed close to the return line to reduce the signal loop area. If necessary, some ground lines should be arranged on the connector as line-to-line isolation. An RC filter is added at the entrance of the control line so as to eliminate the interference in the transmission.

Noting the clock

Clock signal line is the most prone to electromagnetic radiation interference, the alignment should be close to the ground circuit. Crystal oscillator, resonator and oscillator module layout are as close as possible to the processor, usually underneath the ground plane or the shell of the crossed hatched line is connected to the ground plane of the circuit through a short conductor.

It is best to use a crystal oscillator, the harmonic energy is small, after determining the oscillator, do not replace the supplier arbitrarily .

In the clock output line can be connected in series 10 ~ 47Ω damping resistance or application of ferrite beads help to reduce the ring and control the reflection. On all clocked devices, VCC should be decoupled, do not share the same integrated circuit with a device with I // O function. Otherwise, the control line or signal line will be modulated by clock noise. Keeping the clock line away from the I / O circuit to prevent unwanted crosstalk.

Pay attention to reset

Most of the interrupt and reset signal operating frequency can not reach the maximum circuit speed, at its input to increase the high-frequency filter can effectively eliminate unwanted reset and interrupt. In the printed circuit board wiring, it should also make these key lines away from other fast conversion circuit and I / O circuit, and away from the edge of the printed circuit board.

Pay attention to the I / O circuit

I / O coupling noise is a major source of EMI problems. High-frequency noise can be directly coupled through the signal path, but also through the power line or ground wire "modulation" indirect coupling and through the parasitic capacitance and crosstalk coupling. The I / O drive circuit should also be placed as close as possible to the printed circuit board connector. The I / O drive circuit should also be placed as close as possible to the printed circuit board connector.

Early and regular testing

An EMI engineering test plan should be developed throughout the design phase, Collecting the relevant information as soon as possible, do not wait until the prototype is completed before the EMI test, Otherwise, not only the progress is affected, costs will grow exponentially. In the launch test or immunity test, you can develop the necessary test software to make the system part of the work or all work. In the case of conditions permitting, simulation testing is also one of the effective way. In short, EMI issues should consider early, early testing, early settlement, so be prepared.

Concluding remarks

Printed circuit board electromagnetic compatibility design is a very skillful work, which require long-term and a large number of accumulated experience and technology, it can not copy and plagiarism. As long as the design strictly follow the basic design criteria and constantly sum up and learn from the past in the development process of experience and lessons, electromagnetic compatibility design problem is not difficult to solve.